Comments and Response

In view of the comments below Applicant respectively requests that the Examiner reconsider the present application including rejected claims 1-14 and 29-63, withdraw the rejections to these claims, and move these claims to allowance. Applicant's amendments to the claims merely clarify the concepts claimed and are not believed to necessitate a new examination. Applicant notes with agreement that claims 15-28 have been canceled without prejudice.

a. Applicant notes with appreciation that the material provided via supplemental information disclosure statement has been considered and that the form 1449 has been signed and a copy returned.

b. The drawings, specifically FIG. 3B is objected to and a label such as "Prior Art" is required. A proposed Amended FIG. 3B with the "Prior Art" label is included with this amendment and Applicant respectfully submits that this objection has been traversed and therefore requests that it be withdrawn.

c Claims 1 – 50 are rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, to make and/or use the invention. Applicant respectfully notes that claims 15-28 have been canceled without prejudice.

The Examiner maintains that: it is not disclosed that the gate electrode portion in the trench is located "such that the insulation film is located between the inner wall surface and the gate electrode" as recited, variously, by claims 1, 3, 34, and 38. In so far as Applicant can appreciate the Examiners concerns, it appears that the Examiner is concerned with referring to the vertical boundary area between the regions 23, 22, 24 and the insulation region 27 as an inner wall surface. It further appears that the Examiner would prefer to refer to this surface or boundary as an outer wall surface. However, Applicant respectfully notes that the boundary has been consistently referred to as an inner wall surface throughout the specification and that from the perspective of

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one in the trench 46 it would reasonably appear as an inner wall surface. In any event since there is only one surface or boundary of interest in this passage that is clearly depicted in numerous figures there is no indefiniteness introduced by this terminology and thus Applicant respectfully requests that the Examiner withdraw this rejection of these claims.

d. Claim 14 recites, "said highly doped first conductivity type region" without providing proper antecedent basis for this element. Applicant respectfully submits that the proposed amendment to claim 1 establishes the requisite antecedent basis for this element and thus requests that the Examiner withdraw this rejection of claim 14.

e. Claim 1-2 and 29 stand rejected under 35 U.S.C. §102 as being anticipated by prior art as admitted in Applicants disclosure. Generally the Examiner refers to Applicants discussion of Prior Art on pages 2 and 3 with reference to FIG. 20-22 and imposes various of these passages on FIG. 3B. Based on this, the Examiner construes FIG. 3B to show "said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and has a gentle peak at a depth greater than a junction depth of said first conductivity type region within said second conductivity type region, by virtue of the partial cancellation of n- and p- dopants near the interface of regions 3 and 4 (see Figure 3B) and the monotonically decreasing As and B dopant concentrations;" Applicant respectfully notes that regions 3 and 4 are elements shown in FIG. 20 and 22 with the corresponding dopant concentration depicted in FIG. 21.

Claim 1 has been amended to further clarify the impurity concentration of the second conductivity type region. Claim 1 now recites wherein said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and wherein said impurity concentration profile of said second conductivity type region, resulting from impurities of a second conductivity type has a gentle peak at a depth that is greater than a junction depth of said first conductivity type region. Applicant is unable to construe FIG 3B as showing or suggesting a gentle peak in the p type dopant distribution. Furthermore there does not

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seem to be any gentle change in the depth direction of the impurity concentration depicted in FIG. 3B. In contrast FIG. 3A shows a gentle peak and as a result of the gentle peak a more gradual or gentle reduction in the concentration in the vicinity of the peak. This may be further contrasted with the sharp peak characteristic shown in FIG. 21. For these reasons Applicant respectfully submits that the Prior Art discussions does not show or suggest the invention as claimed by claim 1. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw this rejection of claim 1 and by virtue of dependency claims 2 and 29.

f. Claims 34-42 and 51-55 stand rejected under 35 U.S.C. §102(e) as being anticipated by Huang (6,110,799). The Examiner maintains that Huang anticipates all elements of claim 34. Specifically, the Examiner maintains that Huang shows "a second trench located in the second conductivity type region and positioned away from the first trench." Claim 34 has been amended to clarify the physical relationships noted in for example FIG 8-10 recite a second trench extending into but not through the second conductivity type region and positioned away from the first trench. Applicant respectfully notes that, in Huang, the trench 34 of FIG. 8 clearly extends into the substrate or first conductivity layer 10 rather than being extending into but not through the second conductivity region (43 in FIG 8G, for example).

Next the Examiner determines that a single buried p+ region 35 in Huang can be divided into two regions given that impurity concentrations vary monotonically according to depth. Given this curious division of one structure into two structures, the Examiner maintains that:

"a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and

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the protrusion region encompasses the second conductivity type doped region;" is anticipated by Huang.

Applicant respectfully disagrees. There is no suggestion in any of the references or specifically in Huang that the buried layer 35 may be viewed as two layers. Furthermore, implantation followed by a drive in step does not necessarily result in a monotonically decreasing concentration. For example, depending on the drive in process particulars the concentration of the implanted dopant may increase and only after a peak then decrease with depth.

In Huang the p+ region or buried layer 35 comes in contact with the n region structurally, whereas, in the present invention, as recited in claim 34, the p+ region (second conductivity type doped region 74 that has an impurity concentration higher than that of the protrusion region 73) comes in contact the n region via a deep p region (second conductivity type protrusion region 73). In Huang the implantation occurs after forming a second trench (22 in Fig. 3 of Huang) with depth sufficient to reach the n region so that a p+ region of high impurity concentration may be formed. In the present application, as shown in Fig. 8G, after forming a second trench 72 with a depth that nominally reaches halfway through the p region 43 (not enough to reach the n region), ions are implanted to form a deep p region 73 via the second trench 72, and then ions are implanted to form a p region 74 of high impurity concentration to obtain electric contact with the deep p region 73. The present invention is different from Huang for this reason. Applicant respectfully submits that these differences are captured with the claim language defining the second trench 72, the second conductivity type doped region 74, and the protrusion region 73.

These differences are non trivial in terms of impact on the final structure. For example in Huang, because the p+ region 35 is formed directly in contact with the N region by implanting ions at high concentration via the second trench 34, leakage at the p+/n junction tends to occur as a result of damage at the time of processing the trench and also as a result of the highly concentrated ion implantation. In light of overcoming such problems, in the present application, the depth, of the second trench, is set to be a less than the depth and nominally half the depth of the p region 43. Furthermore the two

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layers: a deep P region 73 and highly concentrated P region 74 in electric contact are formed to reduce damage in processing or providing the p/n junction surface.

For these reasons Applicant respectfully submits that Huang (6,110,799) does not show or suggest the invention as claimed by claim 34 and by virtue of dependency claims 35-37. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw this rejection under 35 U.S.C. §102(e) of claim 34 and dependent claims 35-37 based on Huang (6,110,799).

Regarding claim 38, the Examiner maintains that " a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer and being in an electrically floating state" is shown by Huang, referring to FIG. 8 and 9 as the portion of 14 to the left of the left most trench (20 in FIG 3). Applicant respectfully notes that this portion of 14 is beyond the active area for the structure of Huang as defined by the mask 12 (see col. 2, lines 1-5) and thus it is unclear what purpose this portion of 14 may be fulfilling and whether it is electrically floating or whatever as Huang is silent and the cross sectional diagrams do not disclose any purpose for this area. The amendment to claim 38 and 40 merely resolves a potential antecedent basis problem between these claims.

For these reasons Applicant respectfully submits that Huang (6,110,799) does not show or suggest the invention as claimed by claim 38 and by virtue of dependency claims 39-42. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw this rejection under 35 U.S.C. §102(e) of claim 38 and dependent claims 39-42 based on Huang (6,110,799).

Regarding claim 51, the Examiner essentially maintains a similar construction of Huang and believes the portion of 14 and 16 to the left of the left most trench anticipate the claimed a second portion of the second semiconductor layer and a second doped region of a first conductivity type located inside the second portion and proximate to the opening of the first trench wherein the second doped region and the second portion of the second trench MOS structure are in an electrically floating state. Applicant notes

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that these regions of Huang are not part of the active area of the Huang structure as discussed above.

For these reasons Applicant respectfully submits that Huang (6,110,799) does not show or suggest the invention as claimed by claim 51 and by virtue of dependency claims 52-55. Therefore Applicant respectfully requests that the Examiner reconsider and withdraw this rejection under 35 U.S.C. §102(e) of claim 51 and dependent claims 52-55 based on Huang (6,110,799).

g. Claims 3-5 and 30 are rejected under 35 U.S.C. §103(a) as being unpatentable over the Prior Art as disclosed by Applicants in view of Huang (6,110,799). Claim 3 has been amended to clarify the structure depicted and defines a semiconductor device that comprises, among other limitations:

a plurality of second trenches formed to extend into but not through said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches;

a second conductivity type protrusion region, which protrudes downwardly, wherein the second conductivity type protrusion region forms a junction that is deeper than a junction of said second conductivity type region, the protrusion region being positioned beneath the second trench; and

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

As noted above with regard to claim 34 the second trenches 34 shown by Huang are not limited to the second conductivity type region 14 but rather extend to the substrate 10 (see Huang FIG. 8-9). As also noted in reference to claim 34 the second conductivity type protrusion region 73 and the second conductivity type highly doped region 74, each as claimed, are not shown or suggested by the buried layer 35 of Huang.

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Since the Prior Art as known to Applicant and the references that have been cited, specifically Huang, do not whether taken alone or in combination show all elements of claim 3 as noted here and in further detail above with reference to claim 34, Applicant respectfully submits that claim 3 and claims dependent thereon, specifically 4-5 as well as 6-10, 30, and 31-32 have not been rendered unpatentable under 35 U.S.C. §103(a). Thus Applicant respectfully requests that the Examiner reconsider claims 3-5 and 30 and withdraw this rejection.

h. Claims 6-10 and 31-32 are rejected under 35 U.S.C. §103(a) as being unpatentable over Prior art as admitted by Applicants over Huang as applied to claim 3 above, and further in view of Yu et al (6,213,869 B1). As discussed above Applicant believes claim 3 is allowable over Prior Art as disclosed by Applicants in view of Huang (6,110,799). Thus these claims would also be allowable by dependency over the same combination of reference material. The Yu reference does not show or suggest taken alone or together with the other reference material the limitations of independent claim 3 and thus claims 6-10 and 31-32 are believed to be allowable. Thus Applicant respectfully requests that the Examiner reconsider and withdraw this rejection of claims 6-10 and 31-32.

i. Claims 11-14 and 33 are rejected under 35 U.S.C. §103(a) as being unpatentable over Prior Art as admitted by Applicants in their disclosure (pages 2-3 and Fig. 22B) in view of So et al (5,895,951). As detailed above, Applicant believes that claim 1 is allowable and these claims depend from claim 1 and thus by virtue of dependency should also be allowable.

The applicable claims are adapted to alleviate electric field issues at an outer peripheral portion of a power or voltage element having high-withstand or breakdown voltage as shown in Fig. 18 in order to minimize space and to lower the cost of the high-withstand voltage element. So et al. teaches a structure for electric-field alleviation at an outer peripheral portion much as depicted as prior art in Fig. 23-24 of the present application. So's patent is about a structure for a power cell. Therefore, it is difficult to consider anticipating the small spaced outer peripheral electric field alleviating structure

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of the present invention as shown in Fig. 18 according to a combination of the prior art and So et al.

Furthermore, an element of the peripheral portion described in So et al, as shown in Figs. 3E – 3G, is formed by 140 of n-type diffusion layer to form a ordinary equipotential ring in addition to ordinary p-type diffusions 130 and 180. Applicant respectfully believes the structure and effects shown in FIG. 18 of the present application are not anticipated, shown or suggested by the combination of the So et al structure and the prior art. Thus Applicant respectfully submits that all limitations of these claims have not been taught or suggested and requests that the Examiner reconsider and withdraw this rejection of claims 11-14 and 33 are rejected under 35 U.S.C. §103(a).

j. Claims 35-36, 43-50 and 56-63 are rejected under 35 U.S.C. §103(a) as being unpatentable over Huang (6,110,799) in view of Prior art as admitted by applicant. As discussed above it is believed that independent claims 34, 38, and 51 are allowable over the references of record. Each of these claims depend from one of claims 34, 38, and 51 and by virtue of dependency should likewise be allowable. Thus Applicant respectfully requests that the Examiner reconsider and withdraw this rejection of these claims 35-36, 43-50 and 56-63 under 35 U.S.C. §103(a) based on these references.

Accordingly, applicant respectfully submits that the claims, as amended, clearly and patentably distinguish over the cited reference of record and as such are to be deemed allowable. No further examination is believed to be required and thus these claims can be moved to allowance. Such allowance is hereby earnestly and respectfully solicited at an early date. If the examiner has any suggestions or comments or questions, calls are welcomed at the phone number below.

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Although it is not anticipated that any fees are due or payable other than indicated on the enclosed petition for a one month extension of time, the Commissioner is hereby authorized to charge any fees that may be required to Deposit Account No. **50-1147**.

Respectfully submitted,

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CLAIMS SHOWING AMENDMENTS

1. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region, having an island shape, formed on the principal surface of said semiconductor substrate, wherein the second conductivity type region has an impurity concentration profile in a depth direction of the semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type region wherein said impurity concentration profile of said second conductivity type region changes gently in the depth direction of the semiconductor substrate and wherein said impurity concentration profile of said second conductivity type region, resulting from impurities of a second conductivity type has a gentle peak at a depth that is greater than a junction depth of said first conductivity type region;

a trench formed in the semiconductor substrate extending from a surface of said first conductivity type region to at least said second conductivity type region on said semiconductor substrate;

an insulation film formed on an inner wall surface of said trench; and

an electrode portion made of polycrystalline silicon filling said trench, such that said insulation film is located between said electrode portion and said inner wall surface.

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3. (Twice Amended) A semiconductor device comprising:

a semiconductor substrate having a principal surface of a first conductivity type;

a second conductivity type region formed on the principal surface of said semiconductor substrate;

a highly doped first conductivity type region formed inside said second conductivity type region;

a plurality of first trenches, each extending from a surface of said highly doped first conductivity type region to reach at least said second conductivity type region on said semiconductor substrate, thereby defining a channel portion on an inner wall surface of each of the first trenches;

an insulation film formed on the inner wall surface of each of the first trenches;

an electrode portion made of polycrystalline silicon filling each of the first trenches such that said insulation film is located between said electrode portion and said inner wall surface;

a plurality of second trenches formed to extend into but not through [inside] said second conductivity type region so that each of the second trenches is positioned between an adjacent pair of said first trenches;

a second conductivity type protrusion region, which protrudes downwardly, wherein the second conductivity type protrusion region forms a junction that is deeper than a junction of said second conductivity type region, the protrusion region being positioned beneath the second trench; and

a second conductivity type highly doped region having an impurity concentration higher than that of the protrusion region, wherein the depth of the second conductivity type highly doped region is less than that of the junction of said protrusion region, the second conductivity type highly doped region is located beneath the second trench, and wherein the protrusion region encompasses the second conductivity type highly doped region.

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34. (Once Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, wherein the trench MOS structure includes:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, thereby a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench;

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second trench extending into but not through [located in] the second conductivity type region and positioned away from the first trench;

a second conductivity type protrusion region having a junction depth that is greater than the junction depth of the second semiconductor layer, the protrusion region being positioned beneath the second trench; and

a second conductivity type doped region that has an impurity concentration higher than that of the protrusion region, wherein the second conductivity type doped region has a diffusion depth that is less than the junction depth of the protrusion region, the second conductivity type doped region is positioned beneath the second trench, and the protrusion region encompasses the second conductivity type doped region; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through the second trench.

38. (Once Amended) A semiconductor device comprising:

a first semiconductor layer of a first conductivity type;

a trench MOS structure formed on the first semiconductor layer, comprising:

a second semiconductor layer of a second conductivity type located on the first semiconductor layer;

a first trench penetrating the second semiconductor layer to the first semiconductor layer;

a first conductivity type doped region located inside the second semiconductor layer and proximate to an inlet portion of the first trench, wherein a channel portion is defined on a sidewall surface of the first trench between the first conductivity type doped region and the first semiconductor layer;

an insulation film located on an inner wall surface of the first trench; and

a gate electrode located in the first trench such that the insulation film is located between the inner wall surface and the gate electrode;

a second conductivity type island located on the first semiconductor layer and adjacent to the second semiconductor layer of the trench MOS structure, the second conductivity type island being isolated from the second semiconductor layer and being in an electrically floating state; and

an upper electrode, which contacts the first conductivity type doped region of the trench MOS structure through a [the] second trench, wherein the upper electrode is isolated from the second conductivity type island.

40. (Once Amended) The semiconductor device according to claim 39, wherein the trench MOS structure further comprises the[a] second trench located in the second conductivity type region and positioned away from the first trench, the protrusion region being positioned beneath the second trench.